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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,417	02/12/2004	B. Arlen Young	ADPT105101	7761

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GUNNISON MCKAY & HODGSON, LLP
GARDEN WEST OFFICE PLAZA, SUITE 220
1900 GARDEN ROAD
MONTEREY, CA 93940

EXAMINER

NGUYEN, TANH Q

ART UNIT PAPER NUMBER

2182

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/779,417

Applicant(s)

YOUNG, B. ARLEN

Examiner

Tanh Q. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 February 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 18, 19 and 22-33 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 18, 19 and 22-33 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 02/12/04
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

Priority

1. The current status of all nonprovisional parent applications and serial number of the copending divisional applications referenced should be included.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 18-19, 22-33 are rejected under 35 U.S.C. 102(b) as being anticipated by **Beal et al. (USP 5,155,845)**.

4. As per claims 18, 27, **Beal** teaches a system [FIG. 4] comprising:

a host adapter [105, 102; 107, 122 - FIG. 4];

a plurality of target devices [109, 111 - FIG. 4] coupled to said host adapter; and

a memory coupled to said host adapter [HOST PROCESSOR MEMORY - FIG.

14; col. 19, lines 46-48], and said memory having stored therein a hardware I/O control block structure [FIG. 17; col. 19, lines 56-60] comprising:

a sister hardware I/O control block field [field 2: LV (local volume) - FIG. 17]; and

a target identification field [field 3a: RV0 (remote volume 0) - FIG. 17] wherein

upon said sister hardware I/O control block field containing a valid value when said

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hardware I/O control block structure is a new hardware I/O control block structure [request packet from host (new hardware I/O control block structure), with field 2 containing a valid value (e.g. 3 for local volume) - FIG. 17], said hardware I/O control block structure is for a mirrored data transaction [col. 20, line 61-col. 21, line 7] using a target device [e.g. disk drive 1 of remote DSC 107: col. 21, lines 3-7], in said plurality of target devices, identified using information in said target identification field [field 3a containing information for identifying the target device [e.g. 1 for remote volume - FIG. 17].

5. As per claims 19, 22-26; 28-33, Beal teaches the hardware I/O control block structure being one of a plurality of hardware I/O control block structures [structures for DEFINE EXTENT, LOCATE RECORD, and WRITE DATA - FIG. 15, FIG. 16, FIG. 17 respectively] in said memory - claims 19, 28;

upon said sister hardware I/O control block field containing an invalid value when said hardware I/O control block structure is a new hardware I/O control block structure [i.e. field 2 containing a phantom volume of DSC 105 having no physical correspondence in disk drives 109: col. 30, lines 49-51], said hardware I/O control block structure is for a non-mirrored data transaction [i.e. transaction with specified disk drive of remote DSC 107 only: col. 30, lines 51-59] - claims 22, 29;

said valid value comprising a valid hardware I/O control block identification number [identification number 3 indicating a valid disk drive on local volume of DSC 105 and that mirrored data transaction is to be performed: col. 21, lines 1-3] - claims 23, 30;

said invalid value comprising a null [nil, having no value, amounting to nothing,

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invalid, zero] identification number [i.e. field 2 containing a phantom volume of DSC 105 having no physical correspondence in disk drives 109: col. 30, lines 49-51] - claims 24, 31;

said mirrored data transaction comprising a read transaction [a read request for a most current image of the virtual volume that has extended dual copy implementation: col. 23, lines 44-52] - claims 25, 32;

said mirrored data transaction comprising a write transaction [col. 21, lines 31-35] - claims 26, 33.

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 18, 22-27, 29-33 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 27-32 of copending **Application No. 10/779,416** (Attorney Docket No. ADPT105103,

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hereinafter AN416). This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claims 27-32 of AN416 contain every element of claims 18, 22-27, 29-33 of the instant application and as such anticipate claims 18, 22-27, 29-33 of the instant application.

“A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). “ ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

8. As per claims 18, 27, AN416 claims a system comprising:

a host adapter;

a plurality of target devices coupled to said host adapter; and

a memory coupled to said host adapter, and said memory having stored therein a hardware I/O control block structure comprising [claim 27, lines 1-11]:

a sister hardware I/O control block field [a mirror field: claim 27, line 15]; and

a target identification field wherein upon said sister hardware I/O control block field containing a valid value when said hardware I/O control block structure is a new hardware I/O control block structure, said hardware I/O control block structure is for a

mirrored data transaction using a target device, in said plurality of target devices, identified using information in said target identification field [claim 27, lines 15-17; claim 28, lines 3-7].

9. As per claims 22-26, 29-33, AN416 claims upon said sister hardware I/O control block field containing an invalid value when said hardware I/O control block structure is a new hardware I/O control block structure, said hardware I/O control block structure is for a non-mirrored data transaction [claim 27, lines 18-20];

said valid value comprising a valid hardware I/O control block identification number [claim 29];

said invalid value comprising a null identification number [claim 30];

said mirrored data transaction comprising a read transaction [claim 32]; and

said mirrored data transaction comprising a write transaction [claim 31].

10. Claims 18-19, 22-33 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3, 7-8, 17 of **U.S. Patent No. 6, 728,791 (USP791)** in view of **Beal et al. (USP 5,155,845)**.

11. As per claims 18, 27, **USP791** claims a system comprising:

a host adapter [claim 17, lines 1-3];

a plurality of target devices coupled to said host adapter [first data storage device: claim 17, lines 10-11; second data storage device: claim 17, line 16]; and

a memory coupled to said host adapter, and said memory having stored therein a

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hardware I/O control block structure [claim 17, lines 2-7, receiving the hardware I/O control block structure by the host adapter] comprising:

a sister hardware I/O control block field [a first mirror hardware I/O control block field: claim 2, lines 4-5]; and

wherein upon said sister hardware I/O control block field containing a valid value [upon determining entry in said first mirror hardware I/O control block field is valid: claim 3, lines 3-5] when said hardware I/O control block structure is a new hardware I/O control block structure [single hardware I/O control block structure: claim 17, line 6],

said hardware I/O control block structure is for a mirrored data transaction using a target device in said plurality of target devices [upon determining entry in said first mirror hardware I/O control block field (of the single hardware I/O control block structure) being valid: claim 3, lines 3-5, generating a second hardware I/O control block (structure) specifying a mirrored data transaction for the second data storage device: claim 3, lines 2-3, 5-7 - hence the hardware I/O control block structure being for a mirrored data transaction using the second data storage device].

USP791, therefore, claims the invention except for the hardware I/O control block structure comprising a target identification field, and except for the target device being identified using information in the target identification field.

Beal teaches a target identification field in a hardware I/O control block structure [field 3a: RV0 (remote volume 0) - FIG. 17] for identifying a target device for a mirrored transaction [e.g. disk drive 1 of remote DSC 107 being identified as the target device for extended dual copy service: col. 21, lines 3-7].

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the hardware I/O control block structure to comprise a target identification field, as is taught by Beal, in order to identify the target device and to distinguish target device information from other information in the hardware I/O control block structure.

12. As per claims 19, 22-26, 28-33, USP791 claims the hardware I/O control block structure being one of a plurality of hardware I/O control block structures [second hardware I/O control block structure: claim 3, line 3];

upon said sister hardware I/O control block field containing an invalid value when said hardware I/O control block structure is a new hardware I/O control block structure, said hardware I/O control block structure is for a non-mirrored data transaction [claim 7];

said valid value comprising a valid hardware I/O control block identification number [claim 8, lines 8-10];

said mirrored data transaction comprising a read transaction [claim 13, lines 6-7];

Beal teaches said invalid value comprising a null [nil, having no value, amounting to nothing, invalid, zero] identification number [i.e. field 2 containing a phantom volume of DSC 105 having no physical correspondence in disk drives 109: col. 30, lines 49-51]; and

said mirrored data transaction comprising a write transaction [col. 21, lines 31-35].

13. Claims 18-19, 22-33 are rejected under the judicially created doctrine of

obviousness-type double patenting as being unpatentable over claims 1-3, 6-7, 16 of **U.S. Patent No. 6, 701,385 (USP385)** in view of **Beal et al. (USP 5,155,845)**.

14. As per claims 18, 27, USP 385 claims a system comprising:

a host adapter [claim 16, lines 1-3];

a plurality of target devices coupled to said host adapter [first data storage device: claim 16, lines 10-11; second data storage device: claim 16, line 18]; and

a memory coupled to said host adapter, and said memory having stored therein a hardware I/O control block structure [claim 16, lines 2-7, receiving the hardware I/O control block structure by the host adapter] comprising:

a sister hardware I/O control block field [a first mirror hardware I/O control block field: claim 2, lines 4-5]; and

wherein upon said sister hardware I/O control block field containing a valid value [upon determining entry in said first mirror hardware I/O control block field is valid: claim 3, lines 3-5] when said hardware I/O control block structure is a new hardware I/O control block structure [single hardware I/O control block structure: claim 16, line 6],

said hardware I/O control block structure is for a mirrored data transaction using a target device in said plurality of target devices [upon determining entry in said first mirror hardware I/O control block field (of the single hardware I/O control block structure) being valid: claim 3, lines 3-5, generating a second hardware I/O control block (structure) specifying a mirrored data transaction for the second data storage device: claim 3, lines 2-3, 5-7 - hence the hardware I/O control block structure being for a mirrored data transaction using the second data storage device].

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USP385, therefore, teaches the invention except for the hardware I/O control block structure comprising a target identification field, and except for the target device being identified using information in the target identification field.

Beal teaches a target identification field in a hardware I/O control block structure [field 3a: RV0 (remote volume 0) - FIG. 17] for identifying a target device for a mirrored transaction [e.g. disk drive 1 of remote DSC 107 being identified as the target device for extended dual copy service: col. 21, lines 3-7].

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the hardware I/O control block structure to comprise a target identification field, as is taught by Beal, in order to identify the target device and to distinguish target device information from other information in the hardware I/O control block structure.

15. As per claims 19, 22-26, 28-33, USP385 teaches the hardware I/O control block structure being one of a plurality of hardware I/O control block structures [second hardware I/O control block structure: claim 3, line 3];

upon said sister hardware I/O control block field containing an invalid value when said hardware I/O control block structure is a new hardware I/O control block structure, said hardware I/O control block structure is for a non-mirrored data transaction [claim 6];

said valid value comprising a valid hardware I/O control block identification number [claim 7, lines 8-10];

said mirrored data transaction comprising a write transaction [claim 3, lines 6-7];

Beal teaches said invalid value comprising a null [nil, having no value, amounting

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to nothing, invalid, zero] identification number [i.e. field 2 containing a phantom volume of DSC 105 having no physical correspondence in disk drives 109: col. 30, lines 49-51]; and

said mirrored data transaction comprising a read transaction [a read request for a most current image of the virtual volume that has extended dual copy implementation: col. 23, lines 44-52].

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Quang Nguyen whose telephone number is (571) 272-4154 and whose e-mail address is tanh.nguyen36@uspto.gov. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin, can be reached on (571) 272-2100. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 for After Final, Official, and Customer Services, or (571) 273-4154 for Draft to the Examiner (please label "PROPOSED" or "DRAFT").

Effective May 1, 2003 are new mailing address is:

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Effective December 1, 2003, hand-carried patent application related incoming correspondences will be to a centralized location.

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11/12/2004

TQN

November 12, 2004